What is claimed is:

1. A circuit for selectively delaying a reference clock signal, comprising:

a phase splitter having a first output and a second output;

a first delay line having a set of output taps, the first delay line being coupled to the first output;

a second delay line having a set of output taps, the second delay line being coupled to the second output;

a first multiplexor coupled to the set of output taps from the first delay line, the first multiplexor providing an output that is coupled to a first storage device;

a second multiplexor coupled to the set of output taps from the second delay line, the second multiplexor providing an output that is coupled to the first storage device; and

means for comparing an output of the first storage device to an input clock signal and generating a first control signal.

2. A circuit of claim 1, wherein the first control signal is coupled to at least one of the first multiplexor and the second multiplexor.

3. A circuit of claim 1, wherein the comparing means comprises a first phase detector.

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4. A circuit of claim 3, wherein the comparing means further comprises a controller coupled to the first phase detector.

5. A circuit of claim 4, wherein the controller generates control signals that are coupled to the first multiplexor and the second multiplexor.

6. A circuit of claim 5, wherein the control signals cause the first multiplexor and the second multiplexor to select an output tap from the respective sets of output taps.

7. A circuit of claim 1, further comprising:

a third multiplexor coupled to the set of output taps from the first delay line, the third multiplexor providing an output that is coupled to a first interpolator circuit;

a fourth multiplexor coupled to the set of output taps from the second delay line, the fourth multiplexor providing an output that is coupled to the first interpolator circuit;

a fifth multiplexor coupled to the set of output taps from the first delay line, the fifth multiplexor providing an output that is coupled to a second interpolator circuit;

a sixth multiplexor coupled to the set of output taps from the second delay line, the sixth multiplexor providing an output that is coupled to the second interpolator circuit;

the first interpolator providing an output that is coupled to a second storage device;

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the second interpolator providing an output that is coupled to the second the second storage device;

the second storage device providing an output that provides a quadrature output clock signal; and

a quadrature control circuit for generating control signals that are coupled to the third multiplexor, the fourth multiplexor, the fifth multiplexor, and the sixth multiplexor.

8. A circuit of claim 7, wherein the control signals generated at the quadrature control circuit cause the third multiplexor, the fourth multiplexor, the fifth multiplexor, and the sixth multiplexor to select an output tap from the respective sets of output taps.

9. A circuit of claim 7, further comprising a phase detector being coupled to the output of the third multiplexor and the output of the fourth multiplexor, the phase detector providing an output that is coupled to the quadrature control circuit.

10. A circuit of claim 9, wherein the quadrature control circuit is further coupled to the first control signal.

11. A circuit of claim 1, wherein the first delay line includes a power control input for receiving a power control signal, wherein the first delay line is further

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configured to power down selected elements of the first delay line responsive to the power control signal;

the second delay line further includes a power control input for receiving the power control signal, wherein the second delay line is further configured to power down selected elements of the second delay line responsive to the power control signal; and

the control circuit includes a power control output for generating the power control signal, wherein the control circuit is further configured to generate the power control signal based upon the first control signal such that unnecessary delay elements in the first and second delay line are disabled.

12. A circuit of claim 11, further comprising means for detecting a cycle boundary of the reference clock signal and for generating a cycle boundary signal.

13. A circuit of claim 12, wherein the cycle boundary signal is coupled to means for generating the first control signal and the power control signal.

14. A circuit of claim 1, wherein each multiplexor comprises a plurality of first level multiplexors coupled to respective output taps, wherein each first level multiplexor generates an output coupled to a second level multiplexor, wherein each first level multiplexor includes a control input for receiving a first control word derived from the first control signal, wherein the second level multiplexor includes a control input for

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receiving a second control word derived from the first control signal, and wherein the plurality of first level multiplexors are connected to the respective sets of output taps such that only one of the first control word and the second control word is changing between switching from one output tap position to a next output tap position.

15. The circuit of claim 14, wherein the output taps comprise at least a first plurality of output taps and a second plurality of output taps, and wherein each consecutive tap of the first plurality of output taps is connected to first inputs of each consecutive multiplexor of the plurality of first level multiplexors starting with a first multiplexor until the last multiplexor is reached, and wherein each consecutive tap of the second plurality of output taps is connected to second inputs of each consecutive multiplexor starting with the last multiplexor of the plurality of first level multiplexor until the first multiplexor is reached.

16. A circuit for selectively delaying a reference clock signal, the circuit comprising:

a phase splitter for receiving a reference clock signal and outputting an in-phase reference signal and a complementary reference signal, where the complementary reference signal is complementary to the in-phase reference signal;

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a first delay line having an input for receiving the in-phase reference signal and a set of output taps for outputting the in-phase reference signal with successively increasing delay;

a first multiplexor (MUX) having a plurality of inputs, each one of the plurality of inputs being coupled to a corresponding one of the set of output taps of the first delay line, the first MUX having a control input for receiving a first control signal for selecting one of the plurality of inputs for coupling to an output of the first MUX;

a second delay line having an input for receiving the complementary reference signal and a set of output taps for outputting the complementary reference signal with successively increasing delay;

a second MUX having a plurality of inputs, each one of the plurality of inputs being coupled to a corresponding one of the set of output taps of the second delay line, the second MUX having a control input for receiving the first control signal for selecting one of the plurality of inputs for coupling to an output of the second MUX;

a first latch having a set input coupled to the output of the first MUX, a reset input coupled to the output of the second MUX, and an output for producing an output clock signal;

a phase detector having a first input for receiving a feedback clock signal corresponding to the output clock signal, a second input for receiving an input clock signal, where the phase detector is configured to output a difference signal at an output of

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the phase detector that indicates a phase relationship between the feedback clock signal and the input clock signal; and

a controller having an input for receiving the difference signal and an output for generating the first control signal, where the controller is configured to adjust the control signal responsive to the difference signal so as to align the feedback clock signal and the input clock signal.

17. The circuit of claim 16, the circuit further comprising:

a third MUX having a plurality of inputs, each one of the plurality of inputs being coupled to a corresponding one of the set of output taps of the first delay line, the third MUX having a control input for receiving a second control signal for selecting one of the plurality of inputs for coupling to an output of the third MUX, wherein the third MUX outputs a delayed version of the selected input from the first delay line;

a fourth MUX having a plurality of inputs, each one of the plurality of inputs being coupled to a corresponding one of the set of output taps of the second delay line, the fourth MUX having a control input for receiving a third control signal for selecting one of the plurality of inputs for coupling to an output of the fourth MUX, wherein the fourth MUX outputs an advanced version of the selected input from the second delay line;

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a first interpolator circuit having a first input coupled to the output of the third MUX, and having a second input coupled to the output of the fourth MUX, and an output for generating a first quadrature signal;

a fifth MUX having a plurality of inputs, each one of the plurality of inputs being coupled to a corresponding one of the set of output taps of the first delay line, the fifth MUX having a control input for receiving a fourth control signal for selecting one of the plurality of inputs for coupling to an output of the fifth MUX, wherein the fifth MUX outputs an advanced version of the selected input from the first delay line;

a sixth MUX having a plurality of inputs, each one of the plurality of inputs being coupled to a corresponding one of the set of output taps of the second delay line, the sixth MUX having a control input for receiving a fifth control signal for selecting one of the plurality of inputs for coupling to an output of the sixth MUX, wherein the sixth MUX outputs a delayed version of the selected input from the second delay line;

a second interpolator circuit having a first input coupled to the output of the fifth MUX, a second input coupled to the output of the sixth MUX, and an output for generating a second quadrature signal;

a second latch having a set input coupled to the output of the first interpolator, a reset input coupled to the output of the second interpolator, and an output for producing a quadrature output clock signal;

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a first flip-flop having a data input coupled to the output of the fourth MUX, a clock input coupled to the output of the third MUX, and a data output for generating a first test signal; and

a quadrature control circuit having a first input for receiving the first control signal, a second input coupled to the data output of the first flip-flop, a first output for generating the second control signal, a second output for generating the third control signal, a third output for generating the fourth control signal, and a fourth output for generating a fifth control signal, where the quadrature control circuit generates the second control signal and the fifth control signal by offsetting the first control signal by a selected offset value in a first direction relative to the magnitude of the first control signal and generates the third control signal and the fourth control signal by offsetting the first control signal by the selected offset value in a second direction that is opposite to the first direction, where the selected offset value is selected by starting with a first value and successively changing the selected offset value until the test signal changes value.

18. The circuit of claim 17, where the quadrature control circuit is further configured to start with a first minimum value for the offset value, and successively increment the selected offset value until the test signal changes value and then decrement the selected offset value.

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19. The circuit of claim 17, where the quadrature control circuit is further configured to start with a maximum value for the offset value and successively decrement the selected offset value until the test signal changes value.

20. The circuit of claim 17, where the quadrature control circuit is integrated with the control circuit.

21. The circuit of claim 17, where the first interpolator circuit further comprises:

a first inverter having an input coupled to the output of the third MUX and an output;

a second inverter having an input coupled to the output of the fourth MUX and an output; and

a third inverter having an input coupled to the outputs of the first and second inverters and an output for generating the first quadrature signal, where the third inverter is a relatively larger device than first and second inverter devices, and wherein the first quadrature signal is a 90-degree signal relative to the output clock signal.

22. The circuit of claim 17, wherein the second interpolator circuit further comprises:

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a fourth inverter having an input coupled to the output of the fifth MUX and an output;

a fifth inverter having an input coupled to the output of the sixth MUX and an output; and

a sixth inverter having an input coupled to the outputs of the fourth and fifth inverters and an output for generating the second quadrature signal, where the sixth inverter is a relatively larger device than the fourth and fifth inverter devices, and wherein the second quadrature signal is 270-degree signal relative to the output clock signal.

23. The circuit of claim 16, wherein:

the first delay line further includes a power control input for receiving a power control signal, where the first delay line is further configured to power down selected elements of the first delay line responsive to the power control signal;

the second delay line further includes a power control input for receiving the power control signal, where the second delay line is further configured to power down selected elements of the second delay line responsive to the power control signal; and

the control circuit includes a power control output for generating the power control signal, where the control circuit is further configured to generate the power control signal based upon the first control signal such that unnecessary delay elements in the first and second delay lines are disabled.

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24. The circuit of claim 16, where the reference clock signal and input clock signal are both configured to have a 50% duty cycle.

25. The circuit of claim 16, further comprising means for detecting a cycle boundary of the reference clock signal and for generating a cycle boundary signal.

26. The circuit of claim 25, wherein the cycle boundary signal is coupled to the controller generating the first control signal, and wherein the controller uses the cycle boundary signal to adjust the first control signal.

27. The circuit of claim 16, wherein each MUX comprises a plurality of first level multiplexors coupled to respective output taps, wherein each first level multiplexor generates an output coupled to a second level multiplexor, wherein each first level multiplexor includes a control input for receiving a first control word derived from the control signal, wherein the second level multiplexor includes a control input for receiving a second control word derived from the control signal, and wherein the first level of multiplexors are connected to the respective sets of output taps such that only one of the first control word and the second control word is changing between switching from one output tap position to a next output tap position.

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27. A method for recovering a clock signal from an input clock signal, comprising the steps of:

converting a reference clock signal into an in-phase reference signal and a complementary reference signal;

delaying the in-phase reference signal and the complementary reference signal;

generating an output clock signal from the delayed in-phase reference signal and the complementary reference signal;

comparing a feedback signal representing the output clock signal to the input clock signal to generate a first control signal; and

adjusting a length of delay for at least one of the in-phase reference signal and the complementary reference signal based upon the control signal.

28. The method of claim 27, further comprising:

comparing the delayed in-phase reference signal and the delayed complementary reference clock signal to generate a test signal;

generating a set of quadrature control signals using the test signal and the first control signal;

selecting the delayed in-phase reference signal and the delayed complementary reference clock signal based on the set of quadrature control signals to generate a first set of signals and a second set of signals;

interpolating between the first set signal to generate a first quadrature signal;

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interpolating between the second set of signals to generate a second quadrature signal; and

generating a quadrature clock signal using the first quadrature signal and the second quadrature signal.

29. The method of claim 27, wherein delaying the in-phase reference signal and the complementary reference signal comprises delaying the in-phase reference signal and the complementary reference signal via at least two delay lines, and wherein the method further comprises:

generating a power control signal for powering down selected elements of the at least two delay lines.

30. The method of claim 29, further comprising:

generating a cycle boundary signal for adjusting the power control signal and the control signal.

31. A method for recovering a clock signal from an input clock signal, the method comprising the steps of:

converting a reference clock signal into an in-phase reference signal and a complementary reference signal;

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successively delaying the in-phase reference clock signal to produce a series of delayed in-phase reference clock signals;

successively delaying the complementary reference clock signal to produce a series of delayed complementary reference clock signals;

selecting a first one of the series of delayed in-phase reference clock signals and a first one of the series of delayed complementary reference clock signals responsive to a first control signal, where the first one of the series of delayed complementary reference clock signals corresponds to the first one of the series of delayed in-phase reference clock signals;

generating an output clock signal by producing a rising edge in the output clock signal responsive to a rising edge in the first one of the series of delayed in-phase reference clock signals and producing a falling edge in the output clock signal responsive to a rising edge in the first one of the series of delayed complementary reference clock signals;

receiving the input clock signal;

comparing the input clock signal to a feedback clock signal related to the output clock signal to produce a difference signal; and

generating the first control signal responsive to the difference signal in order to bring the feedback clock signal into phase with the input clock signal.

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32. The method of claim 31, further comprising generating the reference clock signal to have a correct duty cycle.

33. The method of claim 31, the method further comprising the steps of:

selecting a second one of the series of delayed in-phase reference clock signals responsive to a second control signal;

selecting a second one of the series of delayed complementary reference clock signals responsive to a third control signal;

selecting a third one of the series of delayed in-phase reference clock signals responsive to a fourth control signal;

selecting a fourth one of the series of delayed complementary reference clock signals responsive to a fifth control signal;

sensing a phase relationship between the second one of the series of delayed in-phase reference clock signals and the second one of the series of delayed complementary reference clock signals to produce a test signal;

generating the second, third, fourth and fifth control signals based upon the first control signal and adjusting the second, third, fourth, and fifth control signals until a state change is detected in the test signal;

interpolating between the second one of the series of delayed in-phase reference clock signals and the second one of the series of delayed complementary reference clock signals to produce a first quadrature signal;

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interpolating between the third one of the series of delayed in-phase reference clock signals and the third one of the series of delayed complementary reference clock signals to produce a second quadrature signal; and

generating a quadrature output clock signal using the first quadrature signal and the second quadrature signal.

34. The method of claim 33, where the step of generating the second, third, fourth, and fifth control signals based upon the first control signal and adjusting the second, third, fourth, and fifth control signals until a state change is detected in the test signal further comprises the steps of:

generating the second control signal by offsetting the first control signal value by an offset value in a first direction relative to the magnitude of the first control signal;

generating the third control signal by offsetting the first control signal value by the offset value in a second direction relative to the magnitude of the first control signal;

selecting a first value for the offset value; and

successively changing the offset value until the state change is detected in the test signal.

35. The method of claim 34, where:

the step of selecting a first value for the offset value further comprises selecting a minimum value for the offset value; and

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the step of successively changing the offset value until the state change is detected in the test signal further comprises successively incrementing the offset value until the state change is detected in the test signal and then decrementing the offset value.

36. The method of claim 34, where:

the step of selecting a first value for the offset value further comprises selecting a maximum value for the offset value; and

the step of successively changing the offset value until the state change is detected in the test signal further comprises successively decrementing the offset value until the state change is detected in the test signal.

37. The method of claim 33, where the step of interpolating between the second one of the series of delayed in-phase reference clock signals and the second one of the series of delayed complementary reference clock signals to produce a first quadrature signal further comprises the steps of:

driving an input of a first large driver device with a first small driver device responsive to the second one of the series of delayed in-phase reference clock signals; and

driving the input of the first large driver device with a second small driver device responsive to the second one of the series of delayed complementary reference clock signals.

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38. The method of claim 33, wherein the step of interpolating between the third one of the series of the delayed in-phase reference clock signal and the third one of the series of delayed complementary reference clock signals to produce a second quadrature signal further comprises the steps of:

driving an input of a second larger driver device with a third small driver device responsive to the third one of the series of delayed in-phase reference clock signals; and

driving the input of the second larger driver device with a fourth small driver device responsive to the third one of the series of delayed complementary reference clock signals.

39. The method of claim 33, where the step of sensing a phase relationship between the second one of the series of delayed in-phase reference clock signals and the second one of the series of delayed complementary reference clock signals responsive to a third control signal to produce a test signal further comprises clocking the second one of the series of delayed complementary reference clock signals with the second one of the series of delayed in-phase reference clock signals to obtain the test signal.

40. The method of claim 34, where:

the step of successively delaying the in-phase reference clock signal to produce a series of delayed in-phase reference clock signals further comprises delaying the in-phase

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reference signal with a first series of delay elements to produce the series of delayed in-phase reference clock signals;

the step of successively delaying the complementary reference clock signal to produce a series of delayed complementary reference clock signals further comprises delaying the complementary reference clock signal with a second series of delay elements to produce the series of delayed complementary reference clock signals; and

the method includes the step of disabling unused ones of the first and second series of delay elements.

41. The method of claim 31, where the step of generating a reference clock signal having a correct duty cycle further comprises generating the reference clock signal with a 50% duty cycle.

42. An apparatus for recovering an input clock signal, the apparatus comprising:

means for generating a reference clock signal having a correct duty cycle;

means for converting the reference clock signal into an in-phase reference signal and a complementary reference signal;

means for successively delaying the in-phase reference clock signal to produce a series of delayed in-phase reference clock signals;

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means for successively delaying the complementary reference clock signal to produce a series of delayed complementary reference clock signals;

means for selecting a first one of the series of delayed in-phase reference clock signals and a first one of the series of delayed complementary reference clock signals responsive to a first control signal, where the first one of the series of delayed complementary reference clock signals corresponds to the first one of the series of delayed in-phase reference clock signals;

means for generating an output clock signal by producing a rising edge in the output clock signal responsive to a rising edge in the first one of the series of delayed in-phase reference clock signals and producing a falling edge in the output clock signal responsive to a rising edge in the first one of the series of delayed complementary reference clock signals;

means for receiving the input clock signal;

means for comparing the input clock signal to a feedback clock signal related to the output clock signal to produce a difference signal; and

means for generating the first control signal responsive to the difference signal in order to bring the feedback clock signal into phase with the input clock signal.

43. The apparatus of claim 42, the apparatus further including:

means for selecting a second one of the series of delayed in-phase reference clock signals responsive to a second control signal;

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means for selecting a second one of the series of delayed complementary reference clock signals responsive to a third control signal;

means for sensing a phase relationship between the second one of the series of delayed in-phase reference clock signals and the second one of the series of delayed complementary reference clock signals responsive to the first control signal to produce a test signal;

means for selecting a third one of the series of delayed in-phase reference clock signals responsive to a fourth control signal;

means for selecting a third one of the series of delayed complementary reference clock signals responsive to a fifth control signal;

means for generating the second, third, fourth and fifth control signals based upon the first control signal and adjusting the second and third control signals until a state change is detected in the test signal;

means for interpolating between the second one of the series of delayed in-phase reference clock signals and the second one of the series of delayed complementary reference clock signals to produce a first quadrature signal;

means for interpolating between the third one of the series of delayed in-phase references clock signals and the third one of the series of delayed complementary reference clock signals to produce a second quadrature signal; and

means for producing a quadrature output clock signal using the first quadrature signal and the second quadrature signal.

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44. The apparatus of claim 43, where the means for generating the second, third, fourth, and fifth control signals based upon the first control signal and adjusting the second and third control signals until a state change is detected in the test signal further comprises:

means for generating the second control signal and the fifth control signal by offsetting the first control signal value by an offset value in a first direction relative to the magnitude of the first control signal;

means for generating the third control signal and the fourth control signal by offsetting the first control signal value by the offset value in a second direction relative to the magnitude of the first control signal;

means for selecting a first value for the offset value; and

means for successively changing the offset value until the state change is detected in the test signal.

45. The apparatus of claim 44, where:

the means for selecting a first value for the offset value further comprises means selecting a minimum value for the offset value; and

the means for successively changing the offset value until the state change is detected in the test signal further comprises means for successively incrementing the offset value until the state change is detected in the test signal and then decrementing the offset value; and

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the step of selecting a first value for the offset value further comprises selecting a maximum value for the offset value; and

the step of successively changing the offset value until the state change is detected in the test signal further comprises successively decrementing the offset value until the state change is detected in the test signal.

46. The apparatus of claim 43, where the means for interpolating between the second one of the series of delayed in-phase reference clock signals and the second one of the series of delayed complementary reference clock signals to produce a first quadrature signal further comprises:

means for driving an input of a first large driver device with a first small driver device responsive to the second one of the series of delayed in-phase reference clock signals; and

means for driving the input of the first large driver device with a second small driver device responsive to the second one of the series of delayed complementary reference clock signals.

47. The apparatus of claim 43, where the means for interpolating between the third one of the series of delayed in-phase references clock signals and the third one of the series of delayed complementary reference clock signals to produce a second quadrature signal further comprises:

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means for driving an input of a second large driver device with a third small driver device responsive to the third one of the series of delayed in-phase reference clock signals; and

means for driving the input of the second larger driver device with a fourth small driver device responsive to the third one of the series of delayed complementary reference clock signals.

48. The apparatus of claim 43, where the means for sensing a phase relationship between the second one of the series of delayed in-phase reference clock signals and the second one of the series of delayed complementary reference clock signals responsive to a third control signal to produce a test signal further comprises means for clocking the second one of the series of delayed complementary reference clock signals with the second one of the series of delayed in-phase reference clock signals to obtain the test signal.

49. The apparatus of claim 42, where:

the means for successively delaying the in-phase reference clock signal to produce a series of delayed in-phase reference clock signals further comprises means for delaying the in-phase reference signal with a first series of delay elements to produce the series of delayed in-phase reference clock signals;

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the means for successively delaying the complementary reference clock signal to produce a series of delayed complementary reference clock signals further comprises means for delaying the complementary reference clock signal with a second series of delay elements to produce the series of delayed complementary reference clock signals; and

the apparatus includes means for disabling unused ones of the first and second series of delay elements.

50. The apparatus of claim 42, where the means for generating a reference clock signal having a correct duty cycle further comprises means for generating the reference clock signal with a 50% duty cycle.

51. The apparatus of claim 42, further comprising means for detecting a cycle boundary of the reference clock signal to generate a cycle boundary signal.

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